查询SSM1105供应商

SSM1105V

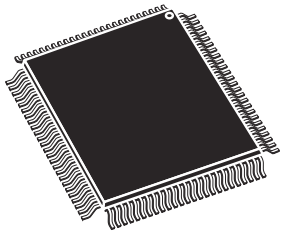
Scalar System Memory (SSM) for Image Processor ICs

NOT FOR NEW DESIGN

FEATURES SUMMARY

- System solution for use with image processing scalar ICs
  - For LCD monitors, projectors, and TVs
  - Compatible with Pixelworks PW11x/PWx64 families (and similar image processors or micro-controllers)
- Single integrated package, including:
  - Dual bank Flash memories
  - DDC, I^2C, and PWM channels
  - General purpose I/O
  - Programmable logic
  - In-System Programming via JTAG
- Dual bank Flash memories
  - Provide concurrent operation
  - 5 Mbit main Flash memory
  - 384 Kbit secondary Flash memory (divided into 10 small sectors)
  - Programmable Decode PLD for flexible address mapping of both memories
- Dual Display Data Channels (DDC)
  - Supports DDC for both analog RGB and digital DVI video input channels
  - DDC1/DDC2B VESA standard compliant
  - 256 byte SRAM buffer for each DDC channel
- Dual independent I^2C channels
  - Each capable of master or slave operation
  - Control A/D converters, video decoders, and future devices (tuner, audio, etc.)
- Four Pulse Width Modulator (PWM) channels
  - 16-bit resolution for period and for duty cycle
  - 16-bit clock prescalers
- Seven I/O ports with 52 I/O pins for Multifunction I/O: GPIO, DDC, I^2C, PWM, PLD I/O, and JTAG
- 3000 gate PLD with 16 macrocells, for creating glue logic, state machines, clock dividers, decoders, chip-selects, inverters; and to prioritize interrupts from DDC, I^2C, PWM

Figure 1. Packages



TQFP100 (U)

- In-System Programming (ISP) with JTAG
  - Program entire chip in 30-40 seconds with no involvement of the processor
  - Program with low-cost FlashLINK
- Content Security: Programmable Security Bit blocks access of device programmers / readers
- Zero-Power Technology: memory and PLD blocks automatically switch to stand-by current between input changes
- Package and Specifications
  - 100-pin TQFP, 14 x 14mm
  - 90 ns memory access time
  - V_{CC} Operating Voltage: 2.7V to 3.6V

This is information on a product still in production but not recommended for new designs.

SUMMARY DESCRIPTION

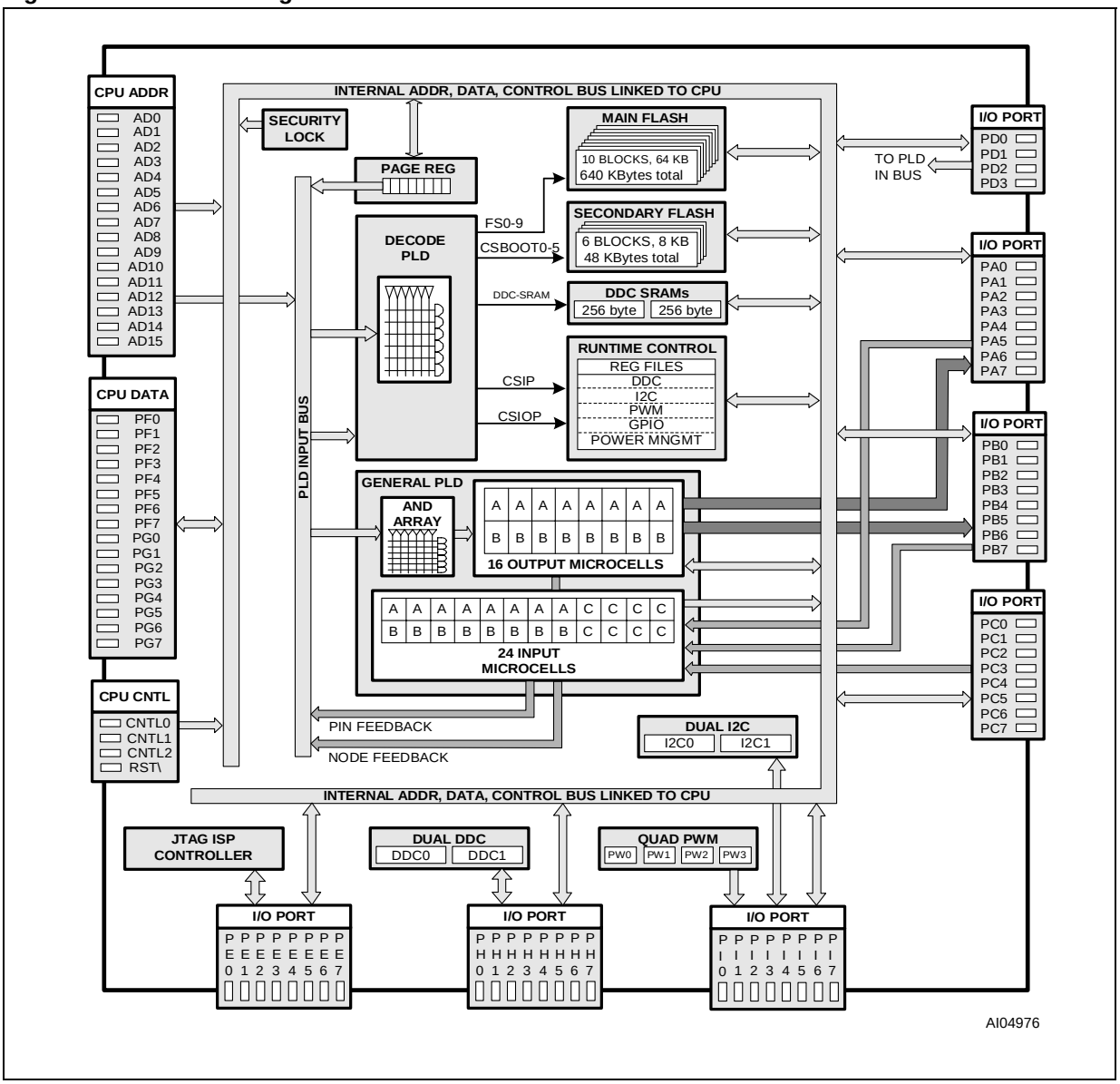
SSM1105V devices bring in-system programmable (ISP) and in-application programmable (IAP) flash memory to LCD monitor, projector and television applications utilizing a scalar IC from either Pixelworks or other similar image processors or micro-controllers (MCU). Figure 3 shows a typical SSM based system with Pixelworks processor.

The SSM1105V devices feature a dual -bank flash architecture, Dual Display Data Channels (DDC), I^2C, PWM channels, general purpose I/O, programmable logic, and in-system programming via either JTAG or I^2C.

The dual-bank Flash memory architecture supports full concurrent operation permitting IAP in the field, which means that firmware can be remotely updated with little interruption of system operation. During run-time, the secondary Flash memory array is ideal for EEPROM emulation, thus eliminating the need for a separate external EEPROM.

An on-chip, decode PLD provides for flexible address mapping for both memories. Dual 256 byte SRAMs provide buffer storage for the DDC channels, thus removing the burden from the processor.

Figure 2. SSM Block Diagram



Note: Additional address lines can be brought in to the device via Port A, B, C or D.

Table 1. Pin Assignments – TQFP100

Pin No.	Pin Assignments
1	PD2
2	PD3
3	GND
4	V_{DD}
5	ADIO0
6	ADIO1
7	ADIO2
8	ADIO3
9	ADIO4
10	ADIO5
11	ADIO6
12	ADIO7
13	ADIO8
14	ADIO9
15	ADIO10
16	ADIO11
17	GND
18	V_{DD}
19	ADIO12
20	ADIO13
21	ADIO14
22	ADIO15
23	$\overline{\text{RESET}}$
24	CNTL2
25	PG0

Pin No.	Pin Assignments
26	PG1
27	PG2
28	PG3
29	PG4
30	PG5
31	PG6
32	PG7
33	PF0
34	PF1
35	PF2
36	PF3
37	PF4
38	PF5
39	PF6
40	PF7
41	V_{DD}
42	GND
43	PH0
44	PH1
45	PH2
46	PH3
47	PH4
48	PH5
49	PH6
50	PH7

Pin No.	Pin Assignments
51	PI0
52	PI1
53	PI2
54	PI3
55	PI4
56	PI5
57	PI6
58	PI7
59	GND
60	V_{DD}
61	PC0
62	PC1
63	PC2
64	PC3
65	PC4
66	PC5
67	PC6
68	PC7
69	GND
70	V_{DD}
71	PA0
72	PA1
73	PA2
74	PA3
75	PA4

Pin No.	Pin Assignments
76	PA5
77	PA6
78	PA7
79	CNTL0
80	CNTL1
81	PB0
82	PB1
83	PB2
84	PB3
85	PB4
86	PB5
87	PB6
88	PB7
89	V_{DD}
90	GND
91	PE0
92	PE1
93	PE2
94	PE3
95	PE4
96	PE5
97	PE6
98	PE7
99	PD0
100	PD1

Figure 3. SSM1105V-Based System Applications

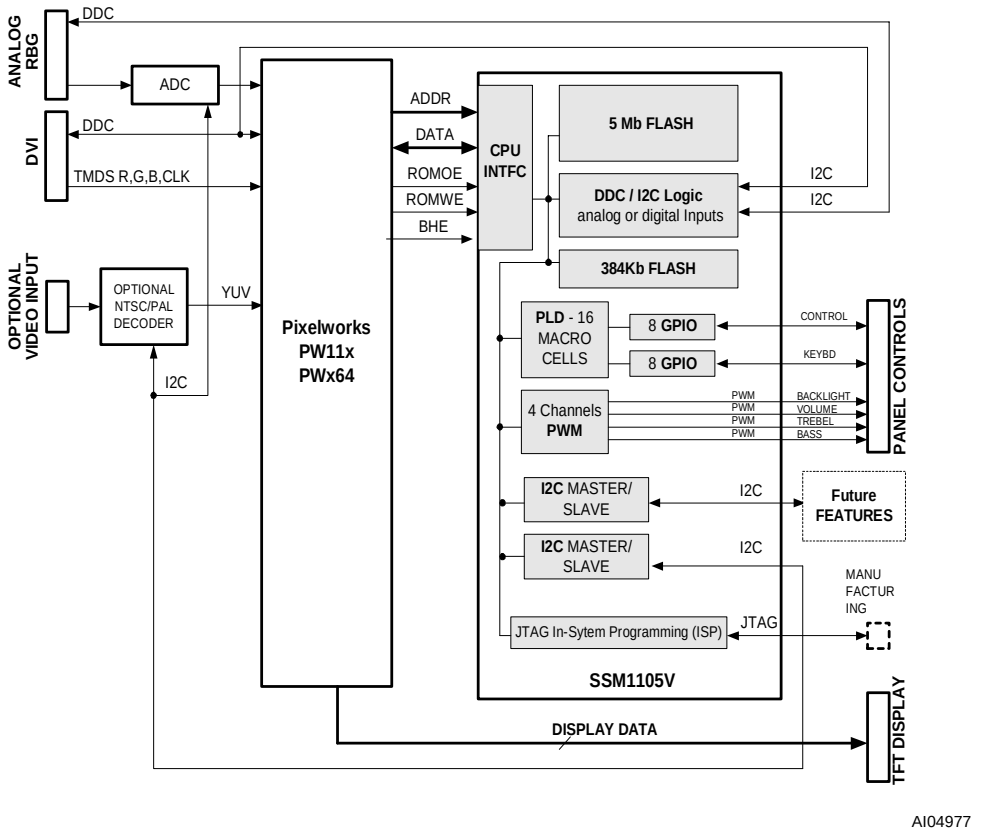


Table 2. Ordering Information Scheme

Example: SSM1105 V – 90 T 1 T

Device Type

SSM1105 = SSM for image processor ICs

Operating Voltage

V = V_{CC} = 2.7 to 3.6V

Speed

90 = 90 ns

Package

T = TQFP100

Temperature Range

1 = 0 to 70 °C (commercial)

Option

T = Tape & Reel Packing